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(54) A method for down-scaling a digital image and a digital camera for processing images of different resolutions

(57) A digital camera for capturing and processing images of different resolutions is described together with a method for down-scaling a digital image. The method comprises the steps of forming an image of a real scene on an image sensor (4) comprising a plurality of pixels arranged in a matrix, addressing and reading pixels in the matrix to obtain analogue quantities related with the pixels luminance values, converting (5) the analogue quantities from the pixels matrix into digital values and processing (6-13) the digital values to obtain a data file representing the image of the real scene. To reduce computation time and power consumption the step of addressing and reading pixels includes the steps of selecting a group of pixels from the matrix, storing the analogue quantities related with the pixels of the selected group of pixels into analogue storing means (14) and averaging the stored analogue quantities to obtain an analogue quantity corresponding to an average pixel luminance value.

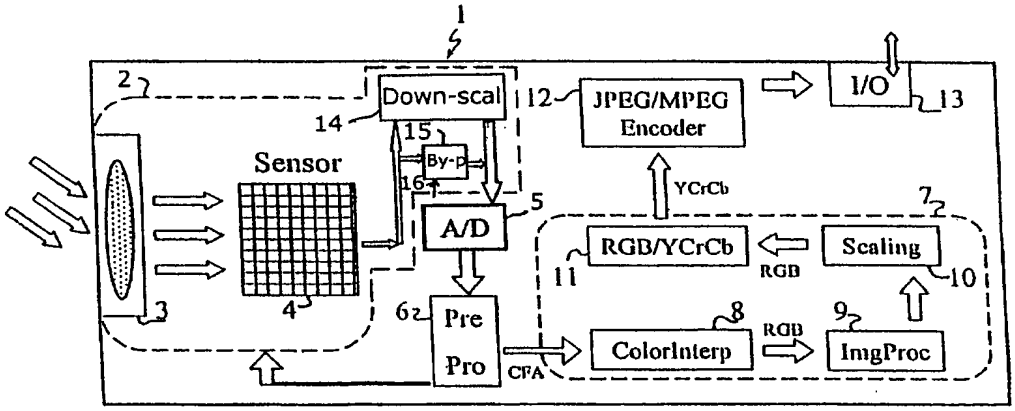

Fig.2

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Description

[0001] The present invention relates to the acquisition and processing of images in digital format and, in particular, to a method for down-scaling a digital image as defined in the preamble of claim 1 and a digital camera for capturing and processing images of different resolutions as defined in the preamble of claim 2.

[0002] Digital still cameras are currently among the most common devices used for acquiring digital images. The ever-increasing resolution of the sensors on the market and the availability of low-consumption digital-signal processors have led to the development of digital cameras which can achieve quality and resolution very similar to those offered by conventional film cameras.

[0003] As well as being able to capture individual images (still pictures), the most recent digital cameras can also acquire video sequences (motion pictures).

[0004] In order to produce a video sequence, it is necessary to acquire a large number of photograms taken at very short intervals (for example 15 photograms per second). The processed and compressed photograms are then encoded into the most common digital video formats (for example MPEG-4).

[0005] In devices which can acquire both individual images and video sequences, there are two conflicting requirements. For photographic applications, high resolution and a large processing capacity are required, even at the expense of acquisition speed and memory occupation. In contrast, for video applications, a fast acquisition speed and optimization of memory resources are required, at the expense of resolution.

[0006] The same remarks are applicable to digital cameras which are not designed for acquiring video sequences in addition to still images, but are provided with a low-resolution digital display for previewing the image before shooting and/or editing images after acquisition.

[0007] With reference to Figure 1, a digital camera 1 for photographic and video applications includes an acquisition block 2 constituted by a lens and diaphragm 3 and by a sensor 4 onto which the lens focuses an image representative of a real scene.

[0008] The sensor 4 is part of an integrated circuit comprising a matrix of photosensitive cells and a driving circuit. Each cell can be addressed and read to obtain an analogue electrical quantity related with the light exposure of the cell.

[0009] The analogue electrical quantity obtained from each photosensitive cell is converted into a digital value by an A/D converter 5. This value may be represented by 8, 10 or 12 bits, according to the dynamics of the camera.

[0010] In a typical sensor, a single photosensitive cell is associated with each pixel. The sensor is covered by an optical filter constituted by a pattern of filter elements each of which is associated with a photosensitive cell. Each filter elements transmits to the photosensitive cell associated therewith the luminous radiation corresponding to the wavelength solely of red light, solely of green light, or solely of blue light (absorbing a minimal portion thereof), so that only one component, that is, the red component, the green component, or the blue component, is detected for each pixel.

[0011] The type of filter used varies according to the manufacturer; the most commonly used is known as a Bayer filter. In this filter, the arrangement of the filter elements, which is known as the Bayer pattern, is shown in Figure 4a in connection with a 6x6 pixel matrix. With a filter of this type, the green component (G) is detected by half of the pixels of the sensor with a chessboard-like arrangement; the red (R) and blue (B) components are detected by the remaining pixels in alternating rows.

[0012] The image output by the analogue/digital converter 5 is an incomplete digital image because it is constituted by a single component (R, G or B) per pixel. The data which represent this image are conventionally referred to as raw CFA (colour filter array)data.

[0013] The raw CFA data are sent to the input of a preprocessing unit (PrePro) 6; this unit is active prior to and during the entire acquisition stage, interacts with the acquisition block 2, and estimates, from the incomplete image, various parameters which are useful for performing automatic control functions, that is: auto-focus, auto-exposure, correction of sensor defects, and white balancing functions.

[0014] The incomplete CFA digital image is then sent to a unit 7 known as the IGP (Image Generation Pipeline) which is composed of several blocks. Starting with the CFA image, a block 8, known as ColourInterp, generates, by means of an interpolation process, a complete RGB digital image in which a set of three components corresponding to the three R, G and B components is associated with each pixel. This conversion may be considered as a transition from a representation of the image in a single plane (Bayer) to a representation in three planes (R, G, B). This image is then processed by a block 9, known as ImgProc, which is provided for improving quality. Several functions are performed in this block 9, that is: exposure correction, filtering of the noise introduced by the sensor 4, application of special effects, and other functions, the number and type of which are variable in general from one manufacturer to another.

[0015] The complete and improved RGB image is passed to a block 10, which is known as the Scaling block. This block reduces the resolution of the image, if required. An application which requires the maximum available resolution equal to that of the sensor (for example a high-resolution photograph) does not require any reduction in resolution. If, however, for example, the resolution is to be halved for acquiring a video sequence, the Scaling block eliminates three quarters of the pixels.

[0016] After scaling, the RGB image is converted by a block 11 into the corresponding YCbCr image, in which each pixel is represented by a luminance component Y

and by two chrominance components Cb and Cr. This is the last step performed in the IGP unit 7.

[0017] The next block is a compression/encoding block 12. Generally, the JPEG format is used for individual images and the MPEG-4 format for video sequences.

[0018] The resolution necessary for video applications or for preview display is lower than that required for photographic applications; nevertheless, in the prior art apparatus, the sensor and the IGP work at maximum resolution in both cases. This leads to wasted computation, which translates into an enormous consumption of time and energy and unnecessary occupation of memory.

[0019] The main object of the invention is to prevent or to limit this problem of the prior art. This object is achieved, according to the invention, by a method and a digital camera as defined and characterised in general in claims 1 and 2, respectively.

[0020] The invention will be better understood from the following detailed description of some embodiments thereof given with reference to the appended drawings, in which:

Figure 1 is a block diagram of a digital camera according to the prior art,
Figure 2 is a block diagram of a digital camera according to the invention,
Figure 3 is a detailed block diagram of a portion of the digital camera according to the invention,
Figures 4a-4f show how the resolution of a digital image is modified by the down-scaling method according to the invention,
Figure 5 is a basic circuit diagram for implementing the down-scaling method of the invention,
Figure 6 is a circuit diagram useful to explain the down-scaling method of the invention,
Figure 7 shows a circuit diagram for down-scaling a 6x6 pixel matrix in a digital camera according to the invention and a table illustrating the operation of the circuit,
Figure 8 is a circuit diagram similar to that of Figure 7 but with a simplified wiring,
Figure 9 shows a simplified version of the circuit diagram of Figure 7 and a corresponding operation table and
Figure 10 is a block diagram representing a generalised down-scaling system of a digital camera according to the invention.

[0021] The block diagram of Figure 2 is similar to that of Figure 1; therefore, reference numerals identical to reference numerals in Figure 1 are used to identify the same or equivalent blocks. A substantial difference in Figure 2 is that the sensor output is not connected to the A/D block 5 directly, but is connected to the A/D block 5 through an analogue down-scaling unit 14 and a block 15 is provided to by-pass the down-scaling unit 14 if a by-pass signal is applied to a control input 16. A digital Scaling block 10 as shown in Figure 1 is included also in Figure 2; however, it can be omitted if a further down-scaling is not required.

[0022] In Figure 3 the sensor 4 is shown in some detail, together with the analogue down-scaling unit 14 and the by-pass block 15. A driver 22 generates clocking signals for addressing each pixel of a sensor matrix 17 at the intersections of row and column lines and transferring pixel signals to a register 23 through the analogue down-scaling unit 14. The analogue signal output by the register 23 is sampled in a sampling block 24 and converted into digital form in the A/D block 5 for further digital processing as explained in connection with Figure 1. A timing generator 25 provides timing signals to a plurality of system units and in particular to driver 22. A microprocessor controller 26 controls the A/D converter 5 and further system units (not shown) and exchanges control signals with the timing generator 25.

[0023] A broad explanation of the operation of the down-scaling method of the invention is given below with reference to Figure 4a-4f. Figure 4a shows a 6x6 pixel matrix of a Bayer patterned pixel array. Figure 4b shows four 3x3 pixel sub-matrices which divide the 6x6 pixel matrix into four quarters Q1-Q4. Figures 4c to 4e show the arrangements of the red (R), green (G) and blue (B) pixels in the matrix of Figure 4a.

[0024] According to the down-scaling method of the invention the four red pixels R in quarter Q4 are detected, an analogue average of the luminance levels of these four pixels is obtained and a new red pixel having this average as its luminance value, as shown at R4 in Figure 4f, is defined. In the same way, the four blue pixels in quarter Q1 are detected and averaged to a new blue pixel B1. The four green pixels at the corners of quarter Q2 and the four green pixels at the corners of quarter Q3 are also detected, an average of each group of four pixels is obtained and two new average green pixels, as shown with G2 and G3 in Figure 4f, are defined. In alternative or in addition, the four green pixels in quarter Q1 and the four green pixels in quarter Q4 can be used to obtain two new average green pixels, as shown with G1 and G4 in Figure 4f.

[0025] Figure 5 shows a preferred implementation of the analogue averaging of four pixels. A 3x3 pixel submatrix 17' has three column lines, indicated as bitlineA, bitlineB and bitlineC, connected to a horizontal register 23' through an averaging unit 14'. A driver unit 22' includes a vertical driver 33, which selects and activates the matrix lines of the matrix 17' by means of control signals sel1, sel2 and sel3, a horizontal driver 34, which generates control signals selA, selB and selC, and a "sample and hold" driver 35, which generates control signals smpl1, smpl2, smpl3 and smpl4. The averaging unit 14' comprises four capacitors C1, C2, C3 and C4 of equal capacitances which have a common terminal and are connectable in parallel to one another by means of three sample and hold switches, S-H2, S-H3 and

S-H4, controlled by signals smpl2, smpl3 and smpl4, respectively. A fourth sample and hold switch S-H1, controlled by signal smpll, is connected to a common terminal N of three switches blA, blB and blC connected to bitline A, bitline B and bitline C, respectively.

[0026] In operation, the drivers 33, 34, 35 generate control signals to activate the matrix rows in sequence and to close and/or open the switches according to a predetermined timing. More particularly, starting from an initial condition with switches blA, blB and blC open and switches SH1, SH2, SH3 and SH4 closed, the timing of the control signals for averaging four pixels of the matrix 17', for example the corner pixels a1, c1, a3, c3, is as follows:

1) sell is high to activate the row line 1, sel2 and sel3 are low,

- selA is high to close switch blA, selB and selC are low,
- the value of pixel a1 is charged into capacitors C1-C4, then
- smpl4 goes low to open switch SH4;

2) with switch SH4 hold open,

- sell is high to activate the row line 1, sel2 and sel3 are low,
- selC is high to close switch blC, selA and selB are low,
- the value of pixel c1 is charged into capacitors C1-C3, then
- smpl3 goes low to open switch SH3;

3) with switches SH4 and SH3 hold open,

- sel3 is high to activate the row line 3, sell and sel2 are low,
- selA is high to close switch blA, selB and selC are low,
- the value of pixel a3 is charged into capacitors C1 and C2, then
- smpl2 goes low to open switch SH2;

4) with switches SH4, SH3 and SH2 hold open,

- sel3 is high to activate the row line 3, sell and sel2 are low,
- selC is high to close switch blC, selA and selB are low,
- the value of pixel C3 is charged into capacitor C1, then
- smpl1 goes low to open switch SH1;

5) now the pixel values of a1, c1, a3, c3 are on capacitors C4, C3, C2, C1 respectively; to perform the averaging, smpl2, smpl3 and smpl4 are set high to turn on the associated switches SH2, SH3 and SH4, thus redistributing the charge between the four capacitors in parallel; the output voltage representing the average luminance level of the four pixels is provided to the horizontal register 23'.

[0027] As is clear to any person skilled in the art of electronic circuit designing, the averaging unit can be implemented in many different ways. In particular, alternative ways of connecting the capacitors to the output of the bitline switching arrangement can be divised, such as to avoid the series connection of the access switches (the sample and hold switches in Figure 5). Furthermore, the capacitors need not to be equal: unequal capacitors can be used advantageously when weighted averaging is required. Moreover, a different number of capacitors can be used according to the number of pixel values to be averaged.

[0028] To perform the down-scaling operation on a 6x6 pixel matrix, a more complex circuit is required. Consider first Figure 6: blA, blB and blC are three column lines of a pixel matrix and NA, NB, NC are three output nodes to be connected each to a bank of four capacitors, as C1-C4 in Figure 5. Each column line blA, blB, blC can be connected to an output node NA, NB, NC either through switches driven by respective signals indicated oA, iA, oB, iB, oC, iC, or through bypass switches driven in common by a signal indicated "bypass". The switches can be driven by a suitable control unit to pass a pixel value from any of the three matrix columns to any of the three capacitor banks connected to the output nodes. For example, to pass a pixel value from column blC to the capacitor bank connected to output node NA, the switches oA and iC are closed, while the remaining switches remain open. The control unit drives the switches so that only one pixel bitline value may be routed to an output node at a time, except when a bypass signal closes the bypass switches; in this case, all other switches are open and the pixels are read as in a normal reading of the pixel matrix at full resolution.

[0029] Consider now a sensor comprising a 6x6 pixel matrix like the Bayer patterned matrix shown in Figure 4a, with columns indicated as A, B, C, D, E, F and rows indicated 1, 2, 3, 4, 5, 6. In the sensor all the pixels in a row share a read access line and all the pixels in a column are connected to a common line (bitline). A circuit for down-scaling the 6x6 Bayer patterned matrix to a 2x2 Bayer patterned matrix with two extra averaged pixels values (like the averaged green pixels in quarters Q1 and Q4 as shown in Figure 4f) is shown in Figure 7. The idealised switches shown in the previous Figures have been replaced by NMOS transistors. The column lines, or bitlines, are indicated blA-blF, the output lines, i.e. the output terminals of the six capacitor banks, are indicated outputA-outputF. The signals for driving the transistors of the capacitor banks are identified by c1-c4 followed by a letter A-F as in the corresponding output line. A switching arrangement similar to the switching arrangement of Figure 6 but using NMOS transistors in place of

switches is connected between the column lines blA-blF and the capacitor banks. The gates of the bypass transistors of the arrangement are connected to a common line for receiving a bypass signal. The control signals applied to the gates of the switching transistors are identified by the letters "o" and "i" followed by a letter A-F as in the corresponding column line blA-blF.

[0030] The sequence of switching operations used to perform the down-scaling as explained above in connection with Figure 4 is given in a table in Figure 7.

[0031] Some sharing between the control signals is possible, so that the wiring required can be reduced, as shown in Figure 8. The pairs of control signals oA and oD, oC and oF, iA and iD, iC and iF are replaced by single control signals oAD, oCF, iAD, iCF, respectively.

[0032] If the extra two green values (G1 and G4) are not necessary, the circuit can be simplified as shown in Figure 9. The switching sequence is given in a table in Figure 9.

[0033] The examples described above use a down-scaling by a factor 3, however the invention can be implemented also for down-scaling by other factors than 3. In general, a down-scaling unit operating according to the method of the invention can be represented by a block diagram as shown in Figure 10. The output lines of a pixel matrix 40 are connected to a plurality of multiplexors 41, which have the same function as the switching arrangements connected to the matrix output lines in Figure 6, for example, and the multiplexor outputs are connected to respective analogue averaging blocks 42 which have the same function as the capacitor banks. The scaled output data from the analogue averaging blocks 42 are then converted in digital form and further processed as explained in connection with Figure 2.

[0034] As is clear from the above description, the object of the invention is fully achieved. In particular, the computation time and the power consumption are greatly reduced because the A/D converter rate is reduced (by 1/6 in the example shown and described) and the amount of pixel data to be processed by the IGP to produce the final image is also reduced (by 1/9 in the example). As a further advantage, the output of the down-scaling unit applied to a Bayer patterned image sensor is itself a Bayer pattern: therefore, both the high and the low resolution outputs can be processed by the same IGP unit. Moreover, the overall system complexity is reduced because the digital scaling circuit can be omitted.

[0035] Although only a few embodiments of the invention have been described, a number of modifications are possible within the scope of the same inventive concept. For example, the inventive method can be applied advantageously to a system comprising a sensor with a filter of a type different from the Bayer filter or also to a monochromatic sensor.

Claims

1. A method for down-scaling a digital image comprising the steps of

   - forming an image of a real scene on an image sensor comprising a plurality of pixels arranged in a matrix,
   - addressing and reading pixels in the matrix to obtain analogue quantities related with the pixels luminance values,
   - converting the analogue quantities from the pixels matrix into digital values,
   - processing the digital values to obtain a data file representing the image of the real scene,

   characterised in that the step of addressing and reading pixels includes the steps of

   - selecting a group of pixels from the matrix,
   - storing the analogue quantities related with the pixels of the selected group of pixels into analogue storing means and
   - producing a weighted average of the stored analogue quantities to obtain an analogue quantity corresponding to an average pixel luminance value.

2. The method of claim 1, wherein the step of producing a weighted average is carried out with equal weights.

3. A digital camera for capturing and processing images of different resolutions comprising:

   - an image sensor (4) comprising a plurality of pixels arranged in a matrix,
   - means (33, 34) for addressing and reading pixels in the matrix to obtain analogue quantities related with the pixel luminance values,
   - means (5) for converting pixel analogue quantities into digital values,
   - means (6, 7, 12, 13) for processing the digital values to obtain a data file representing an image,

   characterised in that it comprises an analogue down-scaling unit (14) and means (15) for bypassing or enabling the down-scaling unit to obtain from the processing means either a high resolution or a low resolution image, respectively, the down-scaling unit (14) including:

   - at least a bank of a predetermined number of capacitive means (C1-C4),
   - means for selecting groups of pixels from the matrix and for charging the capacitive means (C1-C4) of the bank to respective levels corre-

sponding to the analogue quantities of the pixels of a selected group of pixels and

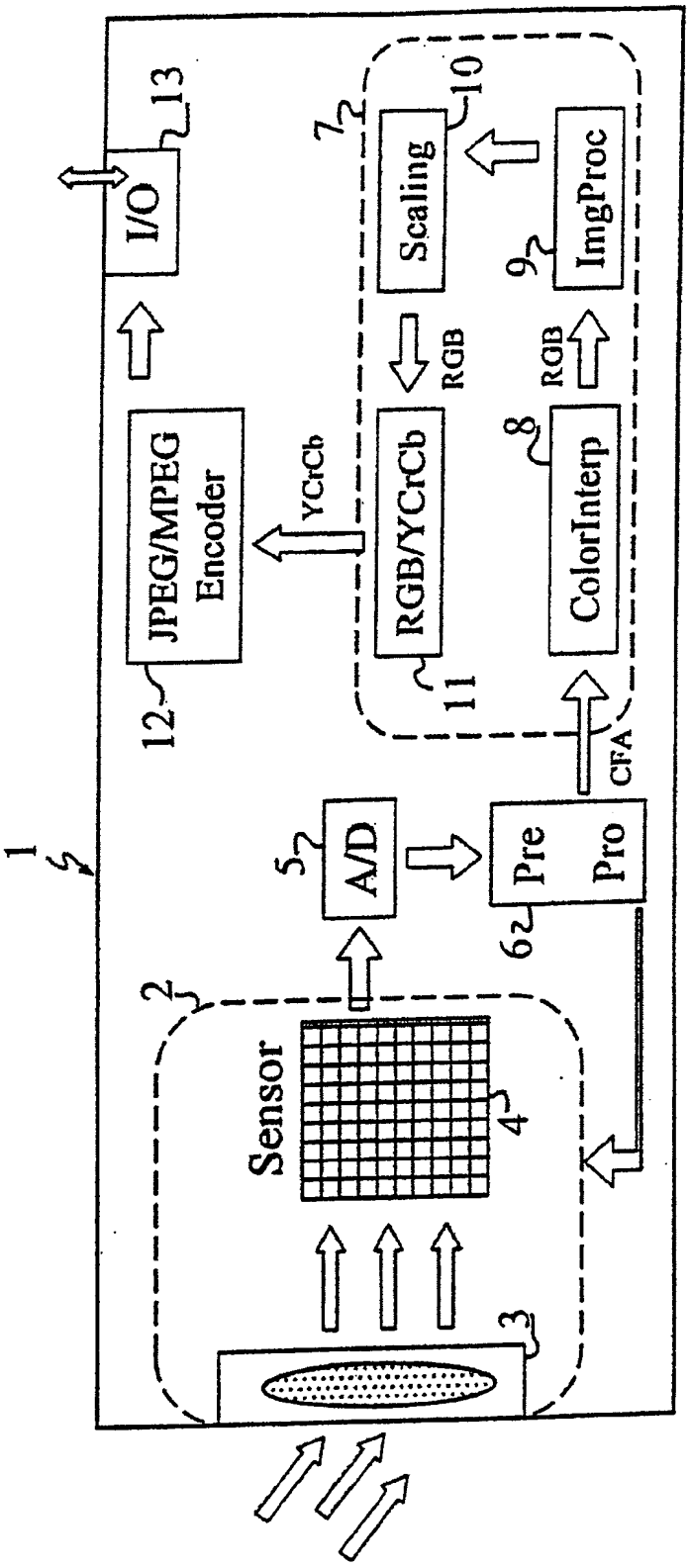
means for producing a weighted average of the charge levels of the capacitive means (C1-C4) of the bank to obtain for each selected group of pixels an analogue quantity corresponding to an average pixel luminance value.

4. The digital camera of claim 3, wherein the capacitive means of at least a bank have equal capacitances and the means for producing a weighted average use equal weights.

5. The digital camera of claim 3 or 4, wherein the pixel matrix is covered by a pattern of colour filters having a predetermined geometrical arrangement.

6. The digital camera of claim 3, 4 or 5, wherein each of the groups of pixels includes four pixels of a 3x3 sub-matrix and each bank of capacitive means includes four capacitive means (C1-C4)

7. The digital camera of claim 6, wherein the means for selecting and charging include row and column line switching means, means for selectively connecting a selected column line to a bank of capacitive means and bank switching means for selectively isolating each of the four capacitive means of the bank.


1
2
Sensor
3
4
5
A/D
6
Pre
Pro
7
8
ColorInterp
CFA
9
ImgProc
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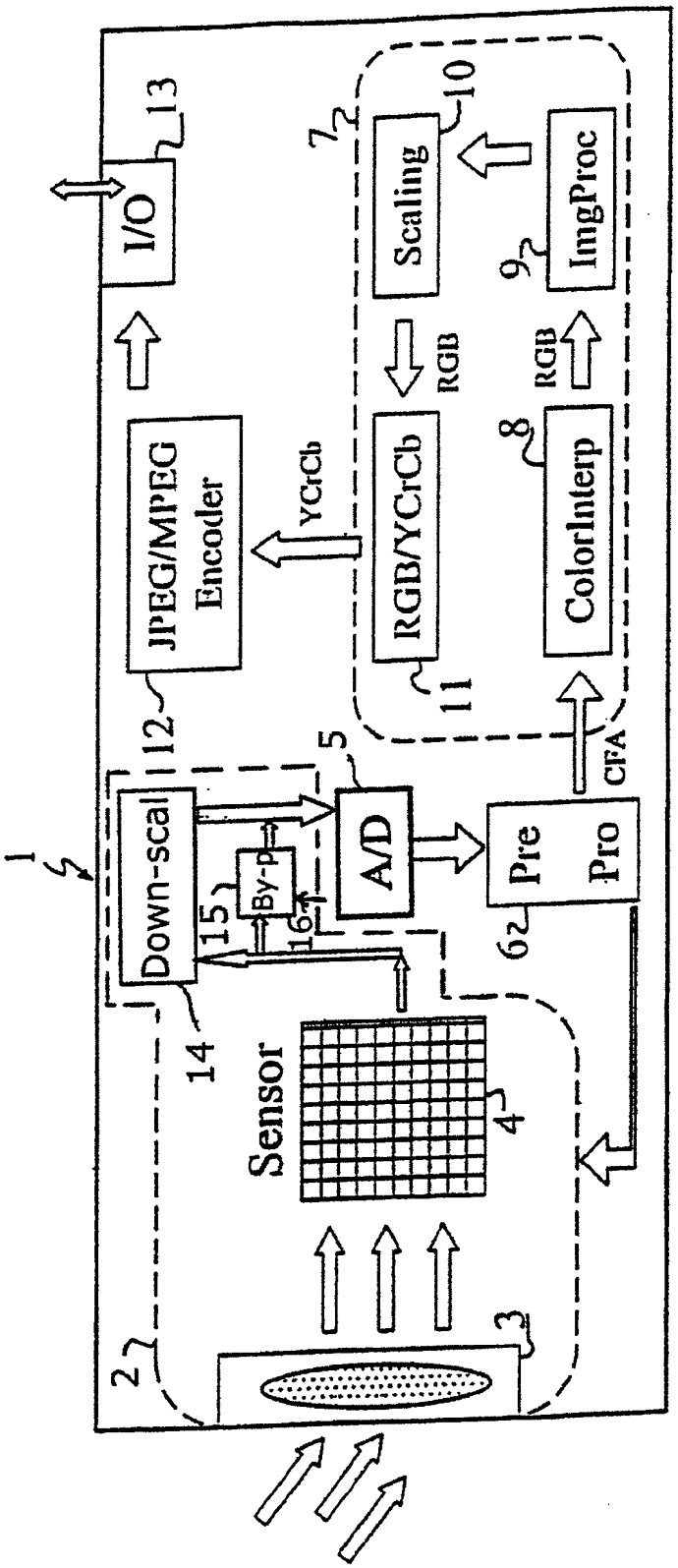
11
RGB/YCrCb
YCrCb
12
JPEG/MPEG
Encoder
13
I/O

Fig.1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4
5
6
7
8
9
10
11
12
13
14
15
16
I/O
JPEG/MPEG Encoder
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ColorInterp
YCrCb
RGB
RGB
CFA

Fig.2

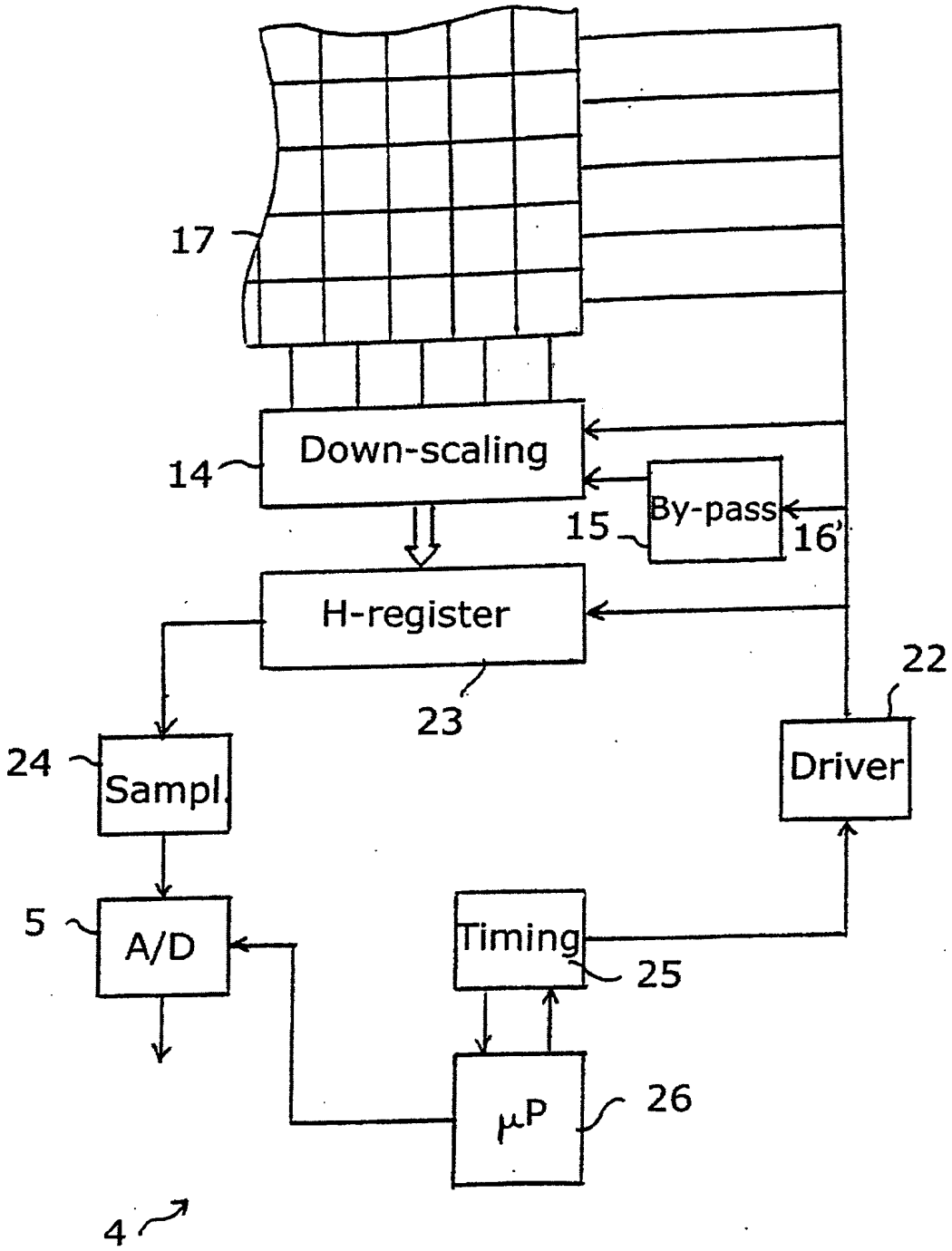

17
Down-scaling
14
By-pass
15
16'
H-register
23
22
Driver
24
Sampl.
5
A/D
Timing
25
μP
26
4

Fig.3

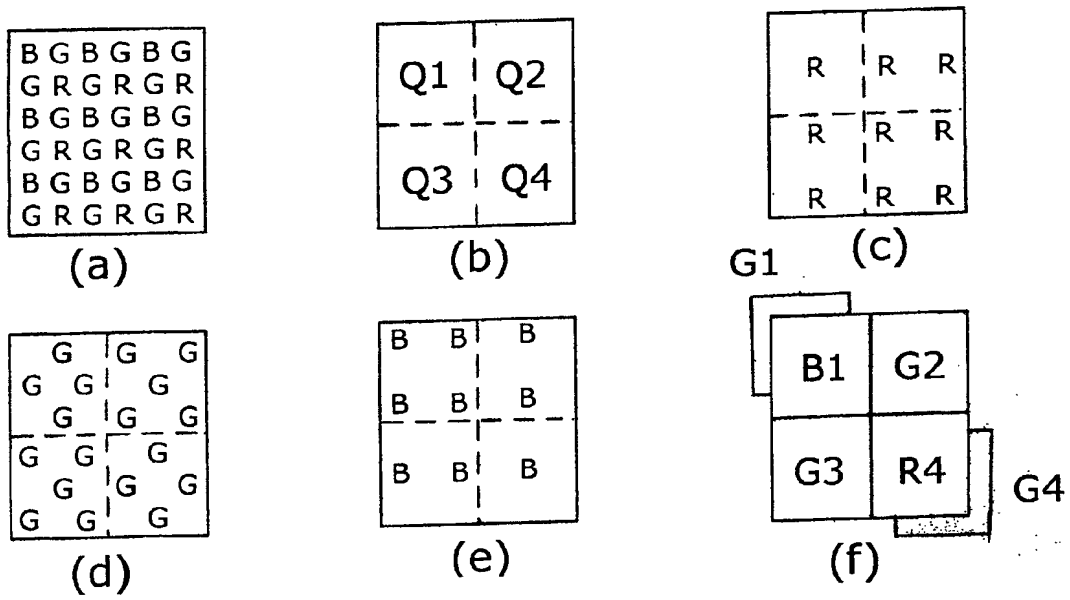

B G B G B G
G R G R G R
B G B G B G
G R G R G R
B G B G B G
G R G R G R
(a)
Q1 Q2
Q3 Q4
(b)
R R R
R R R
R R R
(c)
G1
G G G
G G G
G G G
G G G
G G G
G G G
(d)
B B B
B B B
B B B
(e)
B1 G2
G3 R4
G4
(f)

Fig. 4

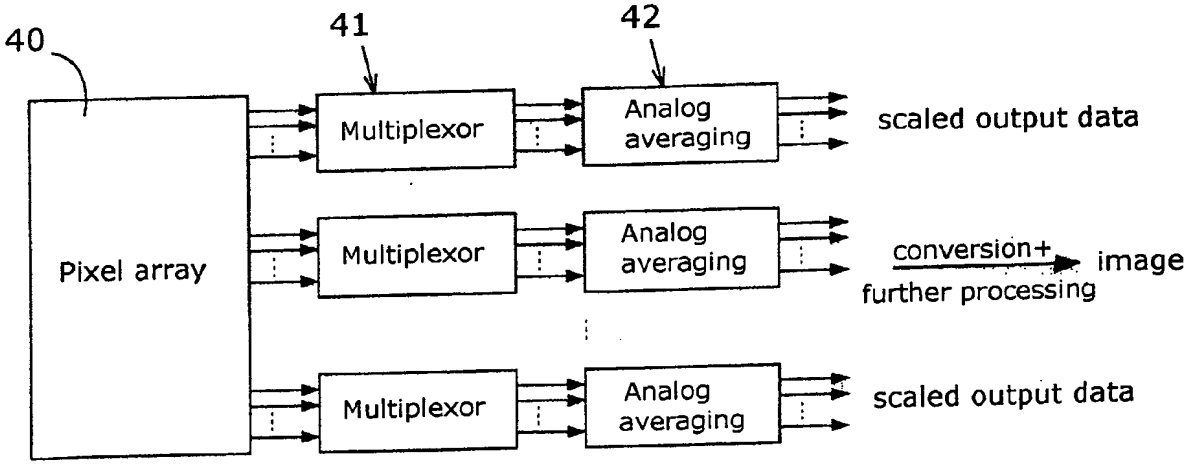
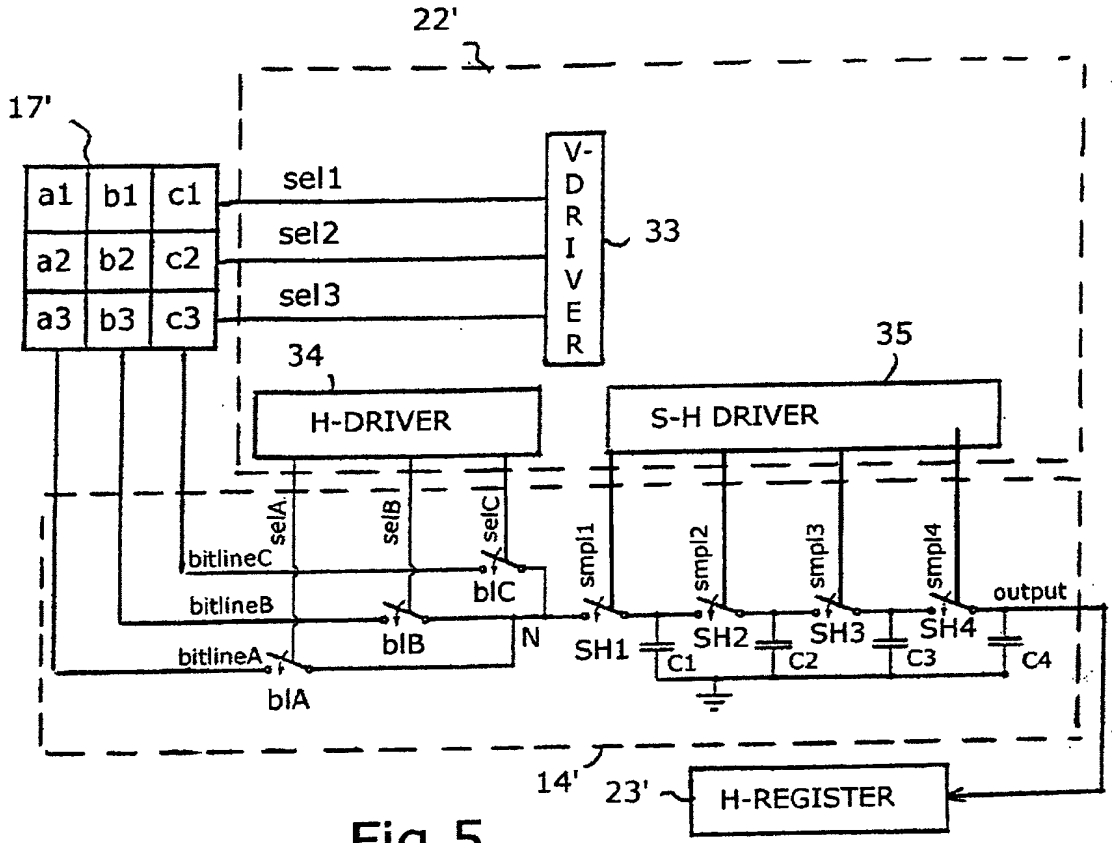

40
41
42
Pixel array
Multiplexor
Multiplexor
Multiplexor
Analog averaging
Analog averaging
Analog averaging
scaled output data
conversion+ further processing
image
scaled output data

Fig. 10


22'
17'
a1
b1
c1
a2
b2
c2
a3
b3
c3
sel1
sel2
sel3
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34
H-DRIVER
35
S-H DRIVER
selA
selB
selC
bitlineC
bitlineB
bitlineA
blC
blB
blA
N
smpl1
smpl2
smpl3
smpl4
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SH3
SH4
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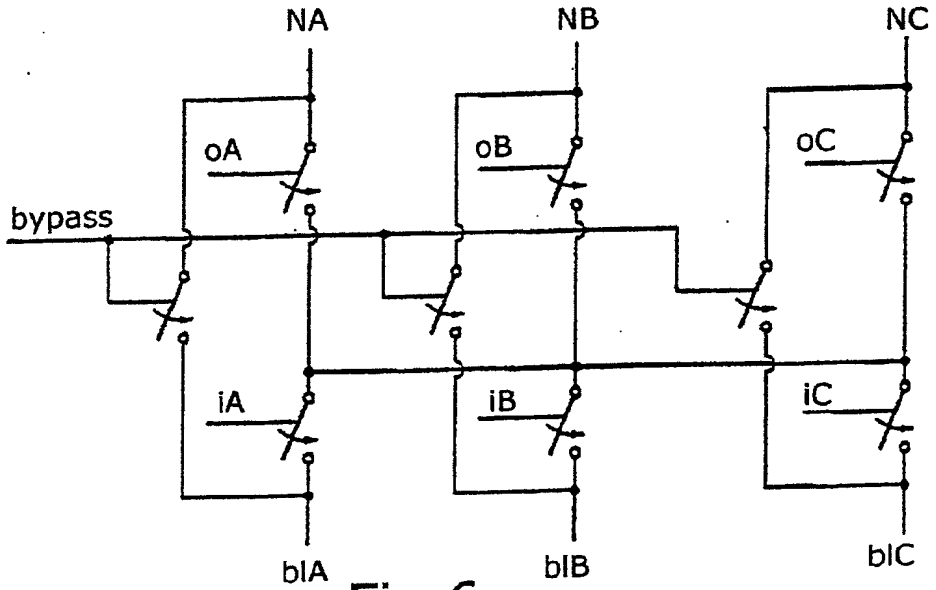
C2
C3
C4
14'
23'
H-REGISTER

Fig.5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NC
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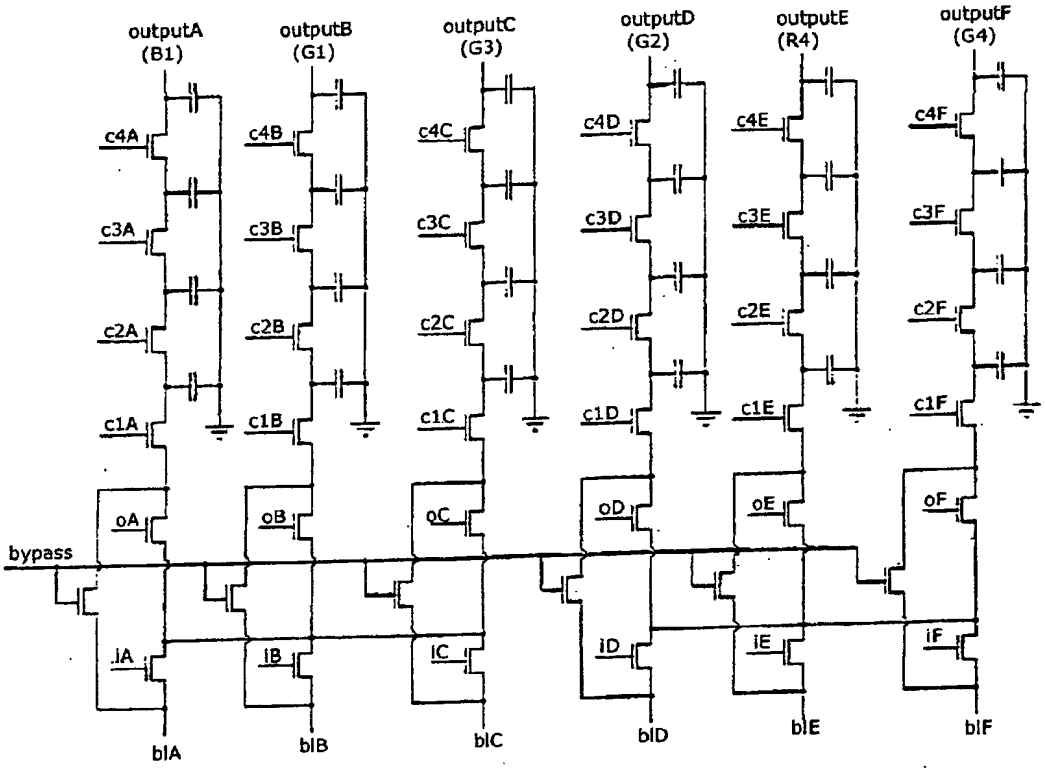
oB
oC
bypass
iA
iB
iC
blA
blB
blC

Fig.6



Pixel row	Columns A-C			Columns D-F		
-	All 'c' switches closed. All other switches open.					
1	iA+oA closed, open c4A	iC+oA closed, open c3A	iB+oB closed, open c4B	iD+oD closed, open c4D	iF+oD closed, open c3D	-
2	iA+oB closed, open c3B	iC+oB closed, open c2B	-	-	-	-
3	iA+oA closed, open c2A	iC+oA closed, open c1A	iB+oB closed, open c1B	iD+oD closed, open c2D	iF+oD closed, open c1D	-
4	iA+oC closed, open c4C	iC+oC closed, open c3C	-	iD+oE closed, open c4E	iF+oE closed, open c3E	iE+oF closed, open c4F
5	-	-	-	iD+oF closed, open c3F	iF+oF closed, open c2F	-
6	iA+oC closed, open c2C	iC+oC closed, open c1C	-	iD+oE closed, open c2E	iF+oE closed, open c1E	iE+oF closed, open c1F
-	All 'i' and 'o' switches open. Close all 'c' switches to average capacitor values.					

Fig.7

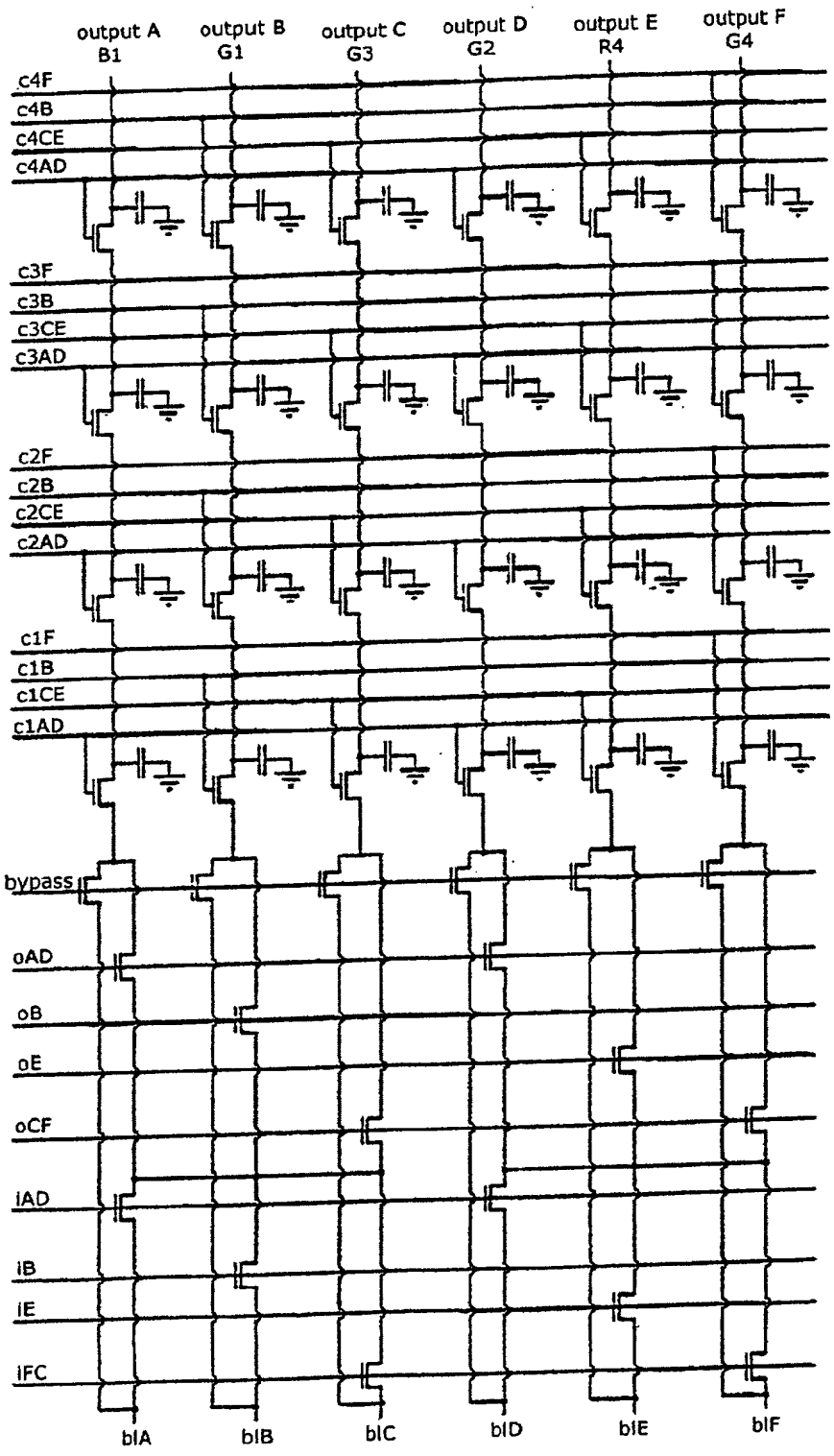
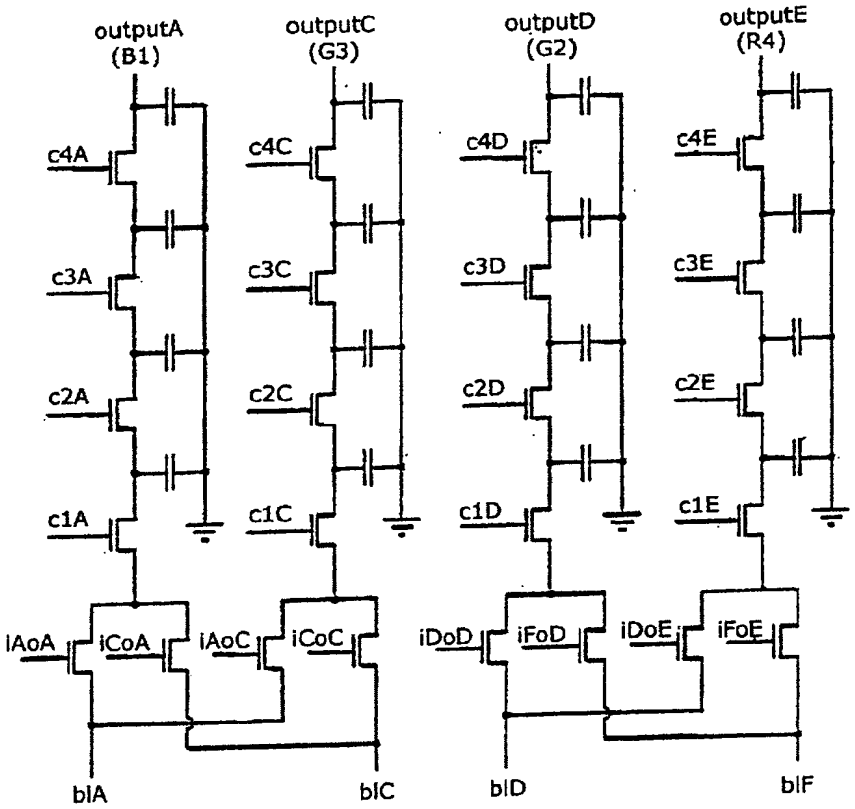

output A
B1
output B
G1
output C
G3
output D
G2
output E
R4
output F
G4
c4F
c4B
c4CE
c4AD
c3F
c3B
c3CE
c3AD
c2F
c2B
c2CE
c2AD
c1F
c1B
c1CE
c1AD
bypass
oAD
oB
oE
oCF
iAD
iB
iE
iFC
blA
blB
blC
blD
blE
blF

Fig. 8



Pixel row	Columns A-C		Columns D-F	
-	All 'c' switches closed. All other switches open.			
1	iAoA closed, open c4A	iCoA closed, open c3A	iDoD closed, open c4D	iFoD closed, open c3D
3	iAoA closed, open c2A	iCoA closed, open c1A	iDoD closed, open c2D	iFoD closed, open c1D
4	iAoC closed, open c4C	iCoC closed, open c3C	iDoE closed, open c4E	iFoE closed, open c3E
6	iAoC closed, open c2C	iCoC closed, open c1C	iDoE closed, open c2E	iFoE closed, open c1E
-	All 'i' and 'o' switches open. Close all 'c' switches to average capacitor values.			

Fig.9

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EUROPEAN SEARCH REPORT

Application Number
EP 02 42 5061

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H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 June 2002	Hardell, A

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